Power Logic 12-CHANNEL SHIFT REGISTER LED DRIVER

Check for Samples: TLC6C5912-Q1

FEATURES

- **Wide V_{CC} From 3 V to 5.5 V**
- **Output Maximum Rating of 40 V**
- **Twelve Power DMOS Transistor Outputs of 50-mA Continuous Current with V_{CC} = 5 V**
- **Thermal Shutdown Protection**
- **Enhanced Cascading for Multiple Stages**
- **All Registers Cleared With Single Input**
- **Low Power Consumption**
- **Slow Switching Time (t_r and t_f), Which Helps Significantly With Reducing EMI**
- **20-Pin TSSOP-PW Package**
- **20-Pin DW Package**

APPLICATIONS

- **Instrumentation Cluster**
- **Tell-Tale Lamps**
- **LED Illumination and Control**

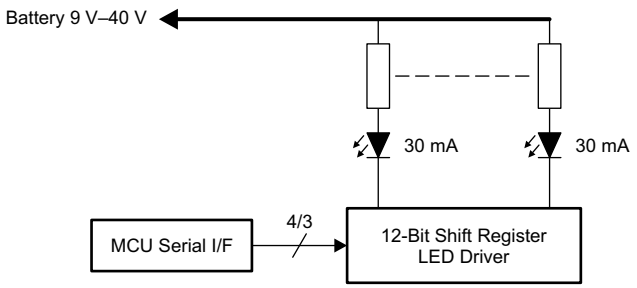


Figure 1. Typical Application Schematic

DESCRIPTION

The TLC6C5912-Q1 is a monolithic, medium-voltage, low-current power 12-bit shift register designed for use in systems that require relatively moderate load power, such as LEDs.

This device contains a 12-bit serial-in, parallel-out shift register that feeds a 12-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift register clear ($\overline{CLR}$) is high. A low on $\overline{CLR}$ clears all registers in the device. Holding the output enable ($\overline{G}$) high holds all data in the output buffers low, and all drain outputs are off. Holding $\overline{G}$ low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability. The serial output (SER OUT) clocks out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This provides improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference. The device contains a built-in thermal shutdown protection.

Outputs are low-side, open-drain DMOS transistors with output ratings of 40 V and 50 mA continuous sink-current capabilities when V_{CC} = 5 V. The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 2000 V of ESD protection when tested using the human-body model and the 200-V machine model.

The TLC6C5912-Q1characterization is for operation over the operating ambient temperature range of −40°C to 125°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LOGIC DIAGRAM (Positive Logic)

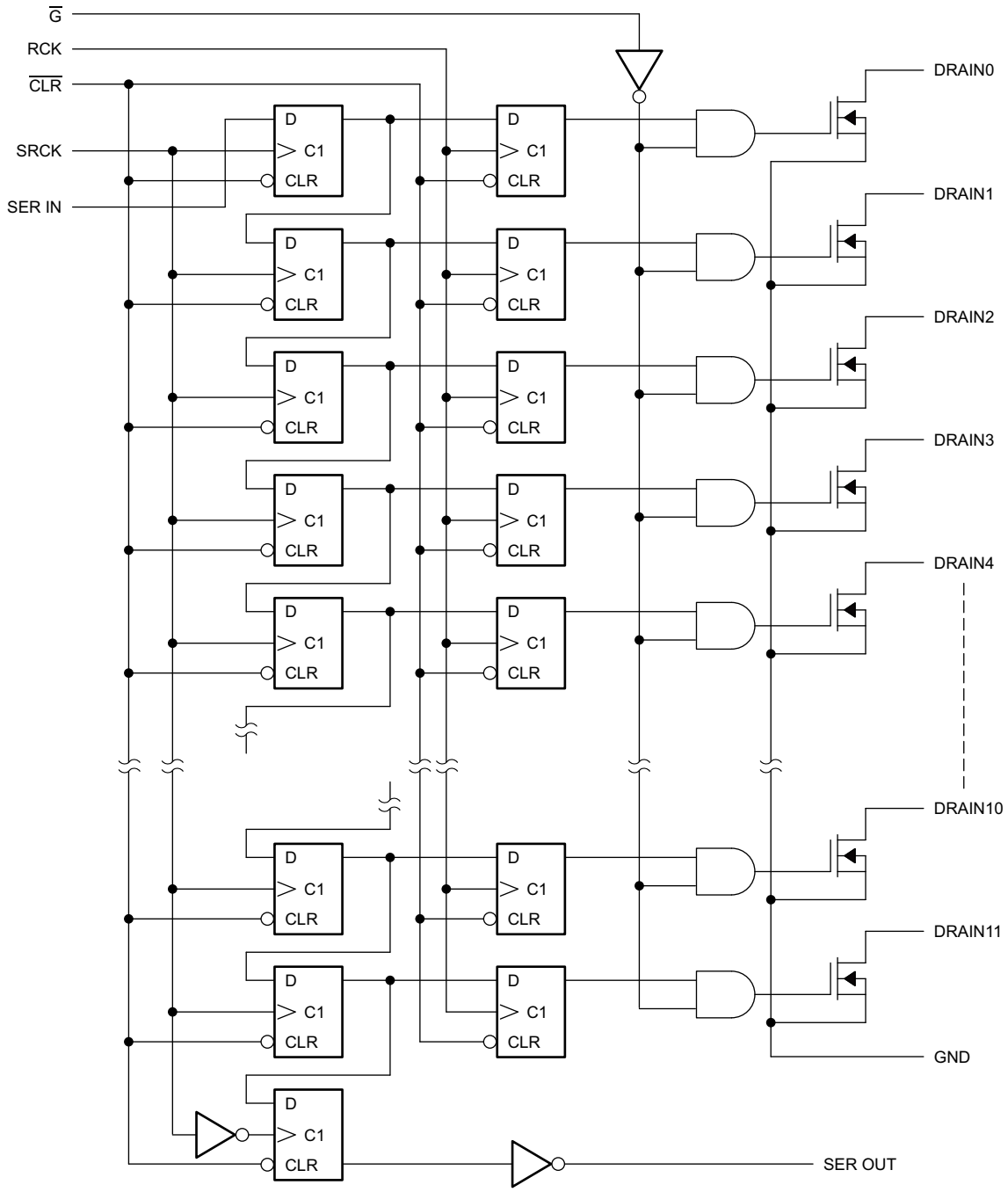


Figure 2. Logic Diagram of TLC6C5912-Q1

ORDERING INFORMATION

LABEL	PACKAGE	DESCRIPTION	ORDERABLE PART#	STATUS
TLC6C5912	TSSOP – PW-20	12-bit shift register LED driver	TLC6C5912QPWRQ1	Active
TLC6C5912	DW-20	12-bit shift register LED driver	TLC6C5912QDWRQ1	Preview

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
V_{CC}	Logic supply voltage		8	V
V_I	Logic input-voltage range		–0.3 to 8	V
V_{DS}	Power DMOS drain-to-source voltage		42	V
	Continuous total dissipation		See Thermal Information table	
	ESD(2)	Electrostatic Discharge HBM	2	kV
	Top	Operating ambient temperature	125	°C
T_S	Storage temperature range		–55 to 165	°C
T_J	Operating junction temperature range		–40 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

THERMAL INFORMATION

THERMAL METRIC(1)		TLC6C5912-Q1		UNIT
		PW	SOIC	
		20 PINS	20 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	114.8	81.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.1	45.4	°C/W
θ_{JB}	Junction-to-board thermal resistance	61.3	49.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.7	17.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.8	48.6	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	5.5	V
V_{IH}	High-level input voltage	2.4		V
V_{IL}	Low-level input voltage		0.7	V
t_{su}	Setup time, SER IN high before SRCK↑	15		ns
t_h	Hold time, SER IN high after SRCK↑	15		ns
t_w	Pulse duration	40		ns
T_C	Operating case temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Drain0 to Drain11. Drain to source voltage					40	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = –20 µA	V_{CC} = 5 V	4.9	4.99		V
		I_{OH} = –4 mA		4.5	4.69		
V_{OL}	Low-level output voltage, SER OUT	I_{OH} = 20 µA	V_{CC} = 5 V		0.001	0.01	V
		I_{OH} = 4 mA			0.25	0.4	
I_{IH}	High-level input current	V_{CC} = 5 V, V_I = V_{CC}			0.2		µA
I_{IL}	Low-level input current	V_{CC} = 5 V, V_I = 0			–0.2		µA
I_{CC}	Logic supply current	V_{CC} = 5 V, No clock signal	All outputs off		0.1	1	µA
			All outputs on		130	170	
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, C_L = 30 pF, all outputs on			300		µA
I_{DSX}	Off-state drain current	V_{DS} = 30 V, V_{CC} = 5 V				0.1	µA
		V_{DS} = 30 V, T_C = 125°C, V_{CC} = 5 V			0.15	0.3	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 20 mA, V_{CC} = 5 V, T_A = 25°C, single channel ON		6	7.4	8.6	Ω
		I_D = 50 mA, V_{CC} = 5 V, T_A = 25°C, all channels ON		6.7	8.9	9.6	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 25°C, single channel ON		7.9	9.3	11.2	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 25°C, all channels ON		8.7	10.6	12.3	
		I_D = 20 mA, V_{CC} = 5 V, T_A = 125°C, single channel ON		9.1	11.2	12.9	
		I_D = 20 mA, V_{CC} = 5 V, T_A = 125°C, all channels ON		10.3	13	14.5	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 125°C, single channel ON		11.6	13.7	16.4	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 125°C, all channels ON		12.8	15.6	18.2	
$T_{SHUTDOWN}$	Thermal shutdown trip point			150	175	200	°C
t_{HYS}	Hysteresis				15		°C

SWITCHING CHARACTERISTICS

V_{CC} = 5 V, T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 48 mA		210		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			75		ns
t_r	Rise time, drain output			250		ns
t_f	Fall time, drain output			200		ns
t_{pd}	Propagation delay time, SRCK↓ to SEROUT	C_L = 30 pF, I_D = 48 mA		35		ns
T_{or}	SEROUT rise time (10% to 90%)	C_L = 30 pF		20		ns
T_{of}	SEROUT fall time (90% to 10%)	C_L = 30 pF		20		ns
$f_{(SRCK)}$	Serial clock frequency	C_L = 30 pF, I_D = 20 mA			10	MHz
T_{SRCK_WH}	SRCK pulse duration, high		30			ns
T_{SRCK_WL}	SRCK pulse duration, low		30			ns

DEVICE INFORMATION

PIN CONFIGURATIONS

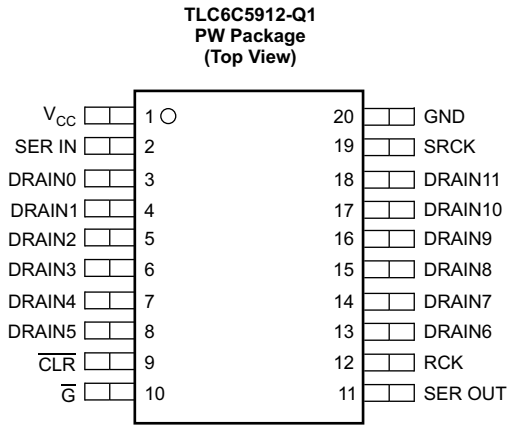


Figure 3. PW-Package Pin Configuration of TLC6C5912-Q1

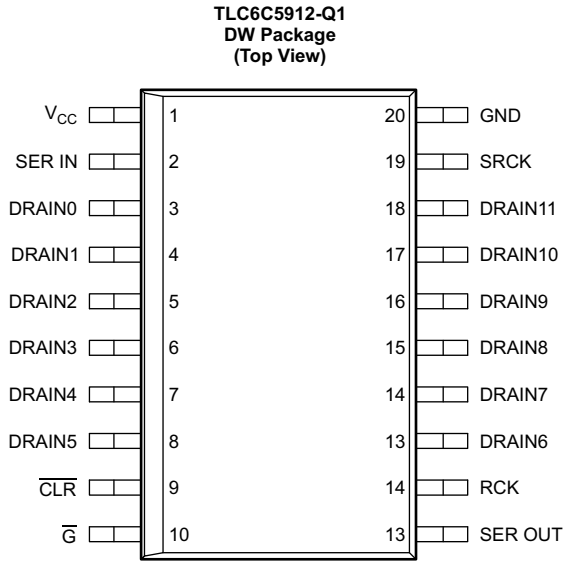


Figure 4. DW-Package Pin Configuration of TLC6C5912-Q1

PIN FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
$\overline{CLR}$	9	I	Shift register clear, active-low
DRAIN0	3	O	Open-drain output
DRAIN1	4	O	Open-drain output
DRAIN2	5	O	Open-drain output
DRAIN3	6	O	Open-drain output
DRAIN4	7	O	Open-drain output
DRAIN5	8	O	Open-drain output
DRAIN6	13	O	Open-drain output
DRAIN7	14	O	Open-drain output
DRAIN8	15	O	Open-drain output
DRAIN9	16	O	Open-drain output
DRAIN10	17	O	Open-drain output
DRAIN11	18	O	Open-drain output
$\overline{G}$	10	I	Output enable, active-low
GND	20	-	Power ground
RCK	12	I	Register clock
SER IN	2	I	Serial-data input
SER OUT	11	O	Serial-data output
SRCK	19	I	Shift-register clock
Vcc	1	I	Power supply

PIN DESCRIPTIONS

$\overline{\text{CLR}}$ is the signal used to clear all the registers. The storage register transfers data to the output buffer when shift register clear $\overline{\text{CLR}}$ is high. Driving $\overline{\text{CLR}}$ is low clears all the registers in the device.

DRAIN0–DRAIN11 are the LED current-sink channels. These pins connect to the LED cathodes, and they can survive up to 40-V LED supply voltage. This is quite helpful during automotive load-dump conditions.

$\overline{\text{G}}$ is the LED channel enable and disable input pin. Having $\overline{\text{G}}$ low enables all drain channels according to the output-latch register content. When high, all channels are off.

GND is the ground reference pin for the device. This pin must connect to the ground plane on the PCB.

RCK is the storage register clock. The data in each shift register stage transfers to the storage register at the rising edge of RCK. Data in the storage register appears at the output whenever the output enable $\overline{\text{G}}$ input signal is high.

SER IN is the serial data input. Data on SER IN loads into the internal register on each rising edge of SRCK.

SER OUT is the serial data output of the 12−bit serial shift register. The purpose of this pin is to cascade several devices on the serial bus. By connecting the SER OUT pin to the SER IN input of the next device on the serial bus to cascade, the data transfers to the next device on the falling edge of SRCK. This can improve the cascade application reliability, as it can avoid the issue that the second device receives SRCK and data input at the same rising edge of SRCK.

SRCK is the serial clock input. On each rising SRCK edge, data transfers from SER IN to the internal serial shift registers.

V_{CC} is the power supply pin voltage for the device. TI recommends adding a 0.1 µF ceramic capacitor close to the pin.

THERMAL SHUTDOWN

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 170°C (typical). The thermal shutdown forces the device to have an open state when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases below 160°C (typical), the device begins to operate again.

APPLICATION INFORMATION

Figure 5 shows a typical cascade application circuit with two TLC6C5912-Q1 chips configured to cascade topology. The MCU generates all the input signals.

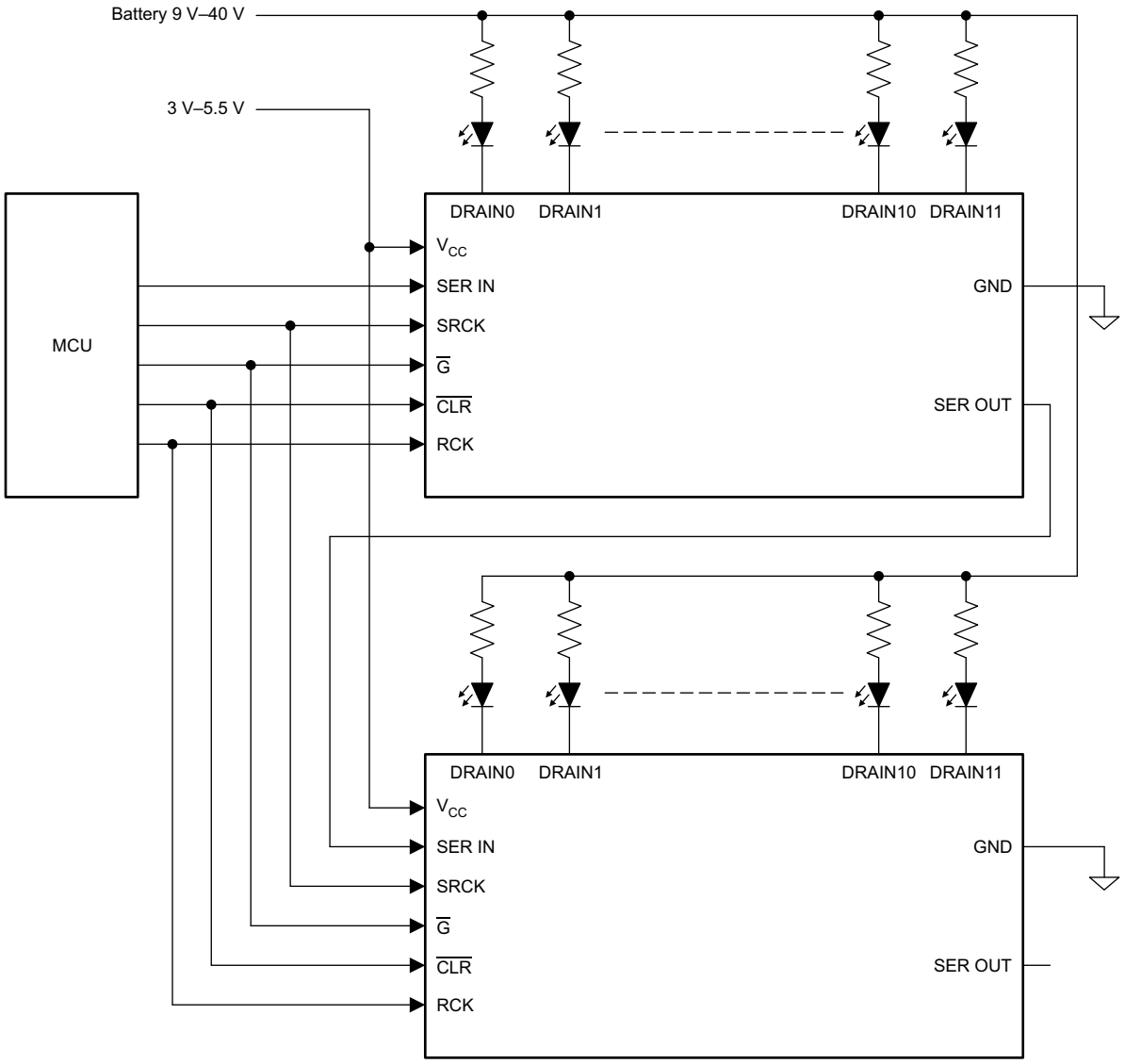
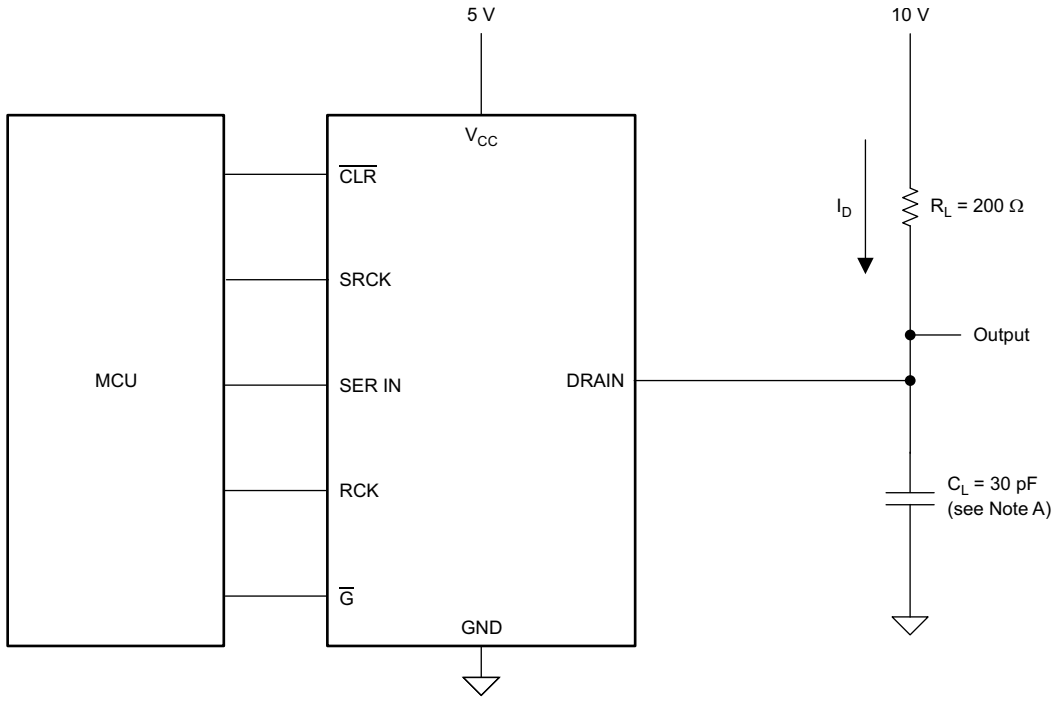


Figure 5. Typical Application Circuit

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 6. Resistive-Load Test Circuit

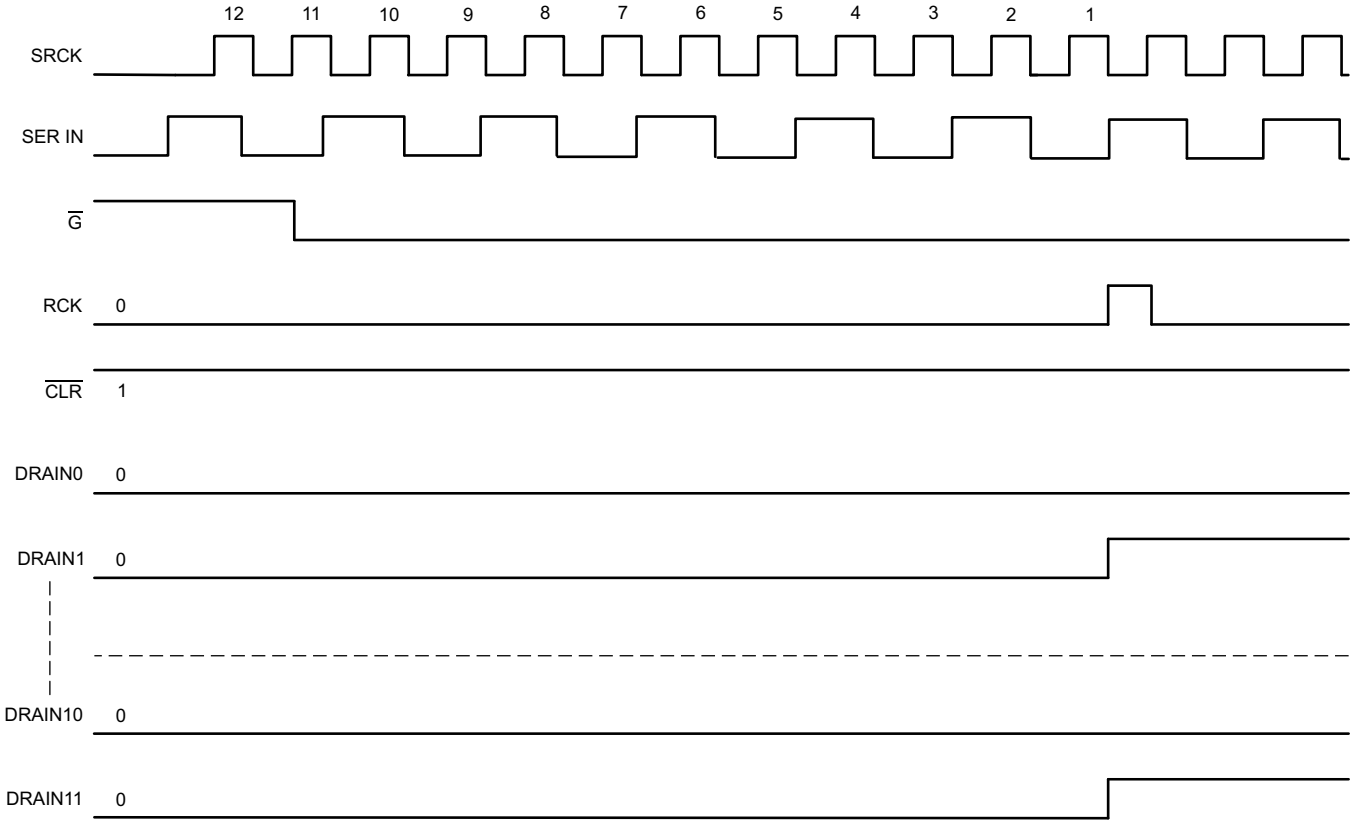


Figure 7. Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

Figure 6 and Figure 7 show the resistive-load test circuit and voltage waveforms. One can see from Figure 7 that with $\overline{G}$ held low and $\overline{CLR}$ held high, the status of each drain changes on the rising edge of the register clock, indicating the transfer of data to the output buffers at that time.

TIMING WAVEFORM

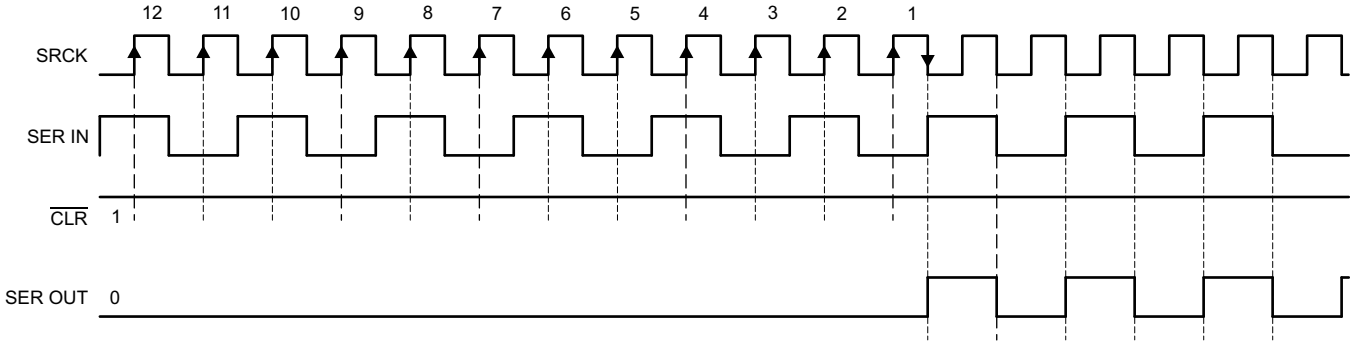


Figure 8. SER IN to SER OUT Waveform

Figure 8 shows the SER IN to SER OUT waveform. The output signal appears on the falling edge of the shift register clock (SRCK) because there is a phase inverter at SER OUT (see Figure 2). As a result, it takes seven and a half periods of SRCK for data to transfer from SER IN to SER OUT.

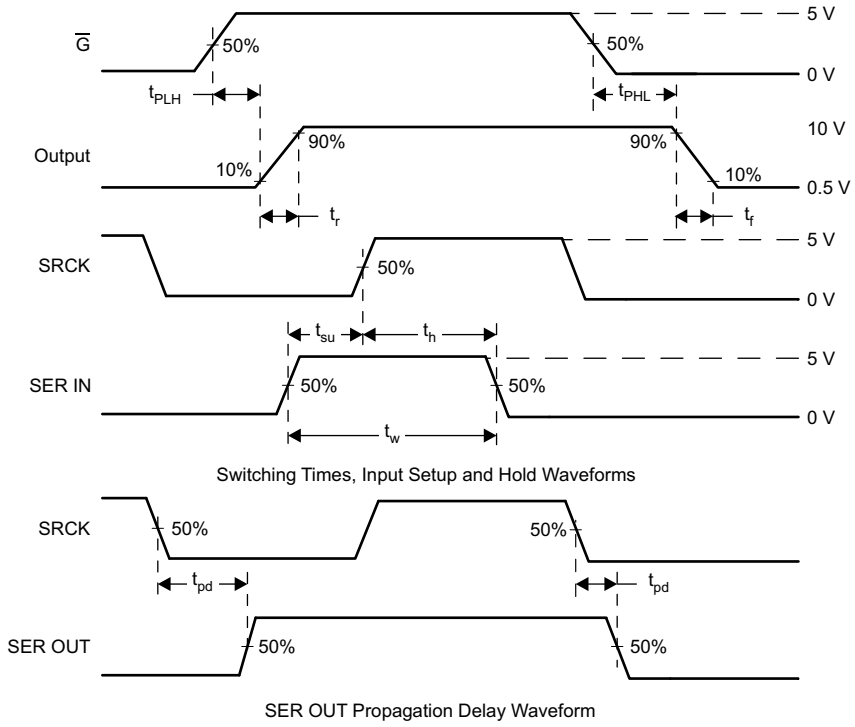


Figure 9. Switching Times and Voltage Waveforms

Figure 9 shows the switching times and voltage waveforms. Tests for all these parameters took place using the test circuit shown in Figure 7.

TYPICAL CHARACTERISTICS

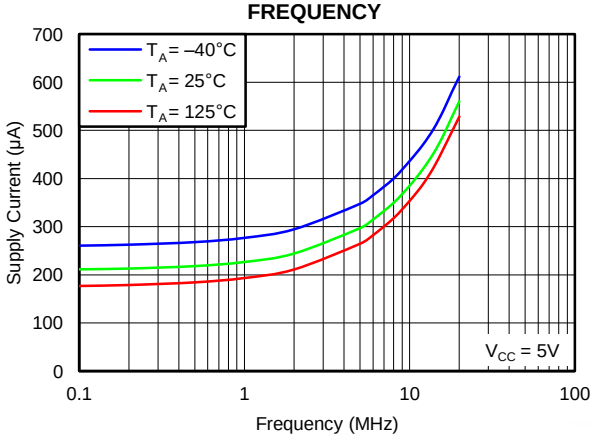


Figure 10.

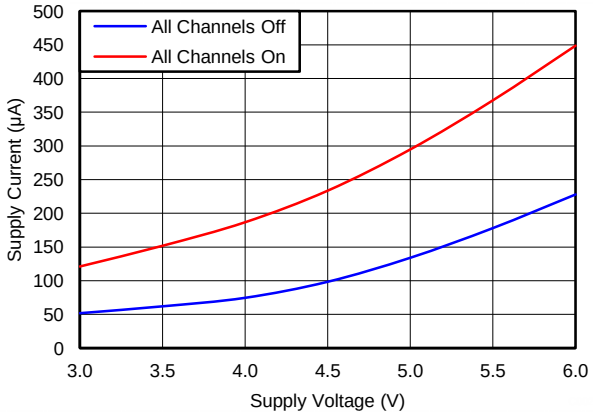


Figure 11.

Conditions for Figure 12 and Figure 13: Single channel on

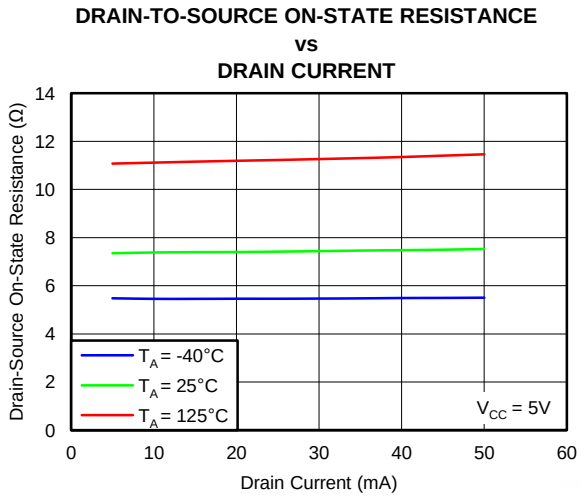


Figure 12.

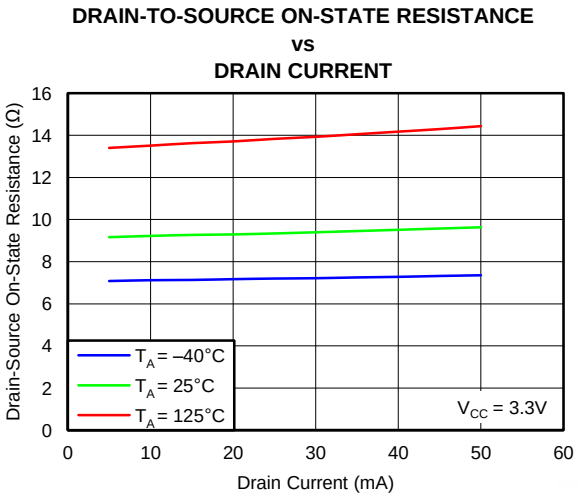


Figure 13.

TYPICAL CHARACTERISTICS

Conditions for Figure 14, Figure 15, and Figure 16: All channels on

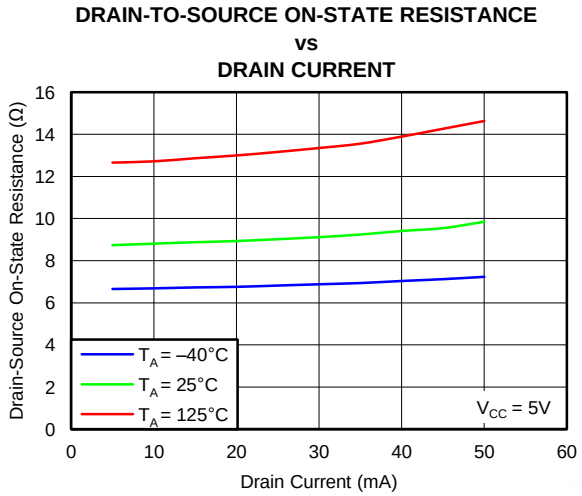


Figure 14.

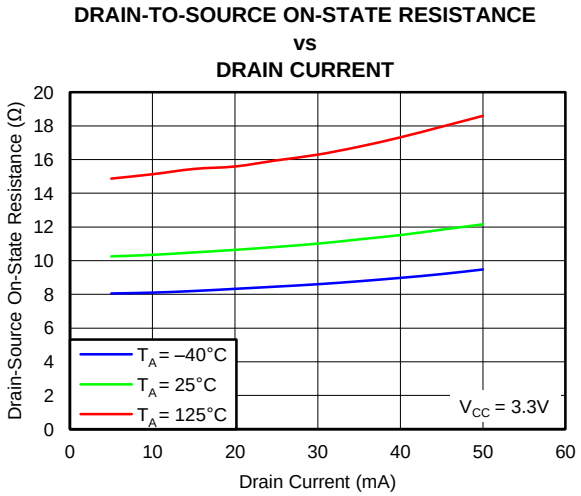


Figure 15.

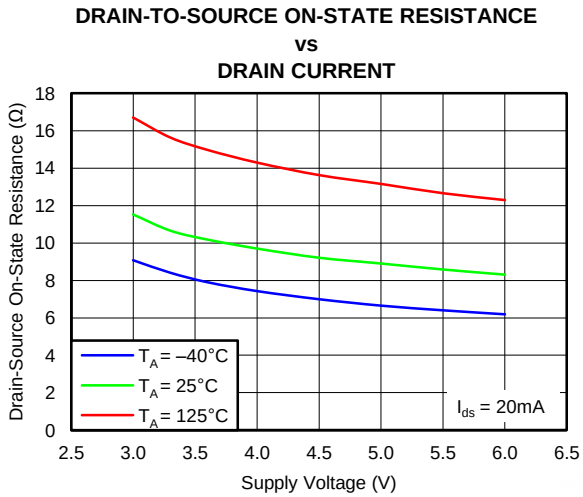


Figure 16.

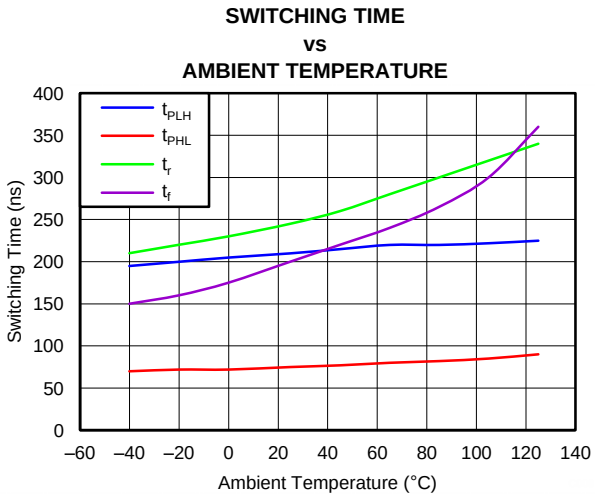


Figure 17.

REVISION HISTORY

Changes from Original (December 2012) to Revision A	Page
• Changed the device From: Product Preview To: Production	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC6C5912QDWRQ1	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TLC6C5912	Samples
TLC6C5912QPWQ1	PREVIEW	TSSOP	PW	20	70	TBD	Call TI	Call TI	-40 to 125		
TLC6C5912QPWRQ1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	6C5912	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

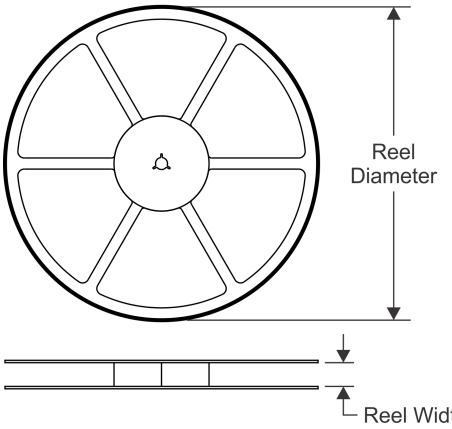
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

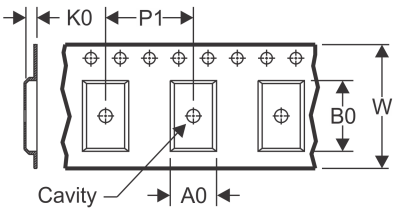
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

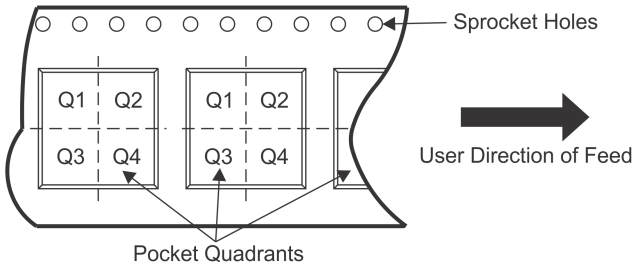


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

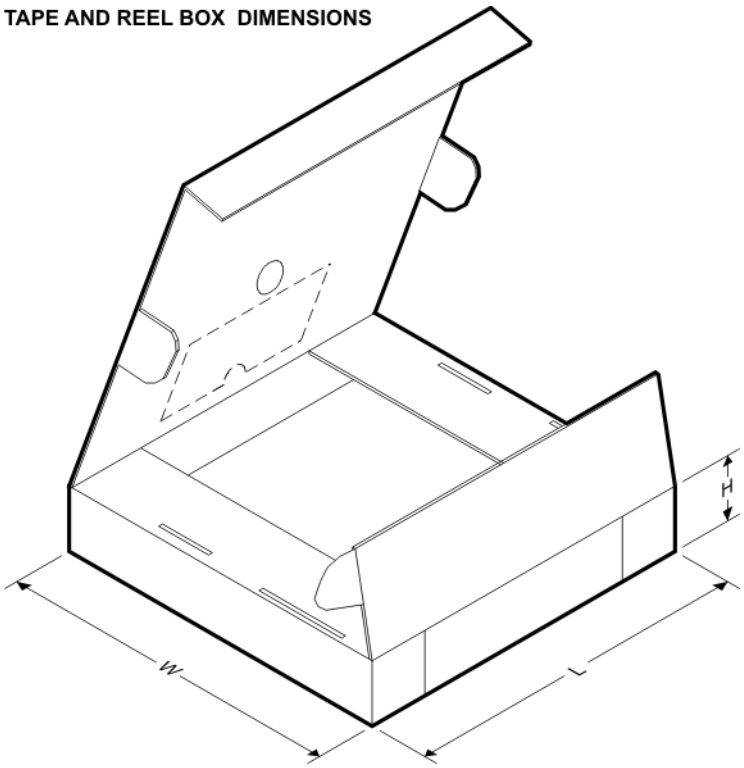
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC6C5912QDWRQ1	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLC6C5912QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

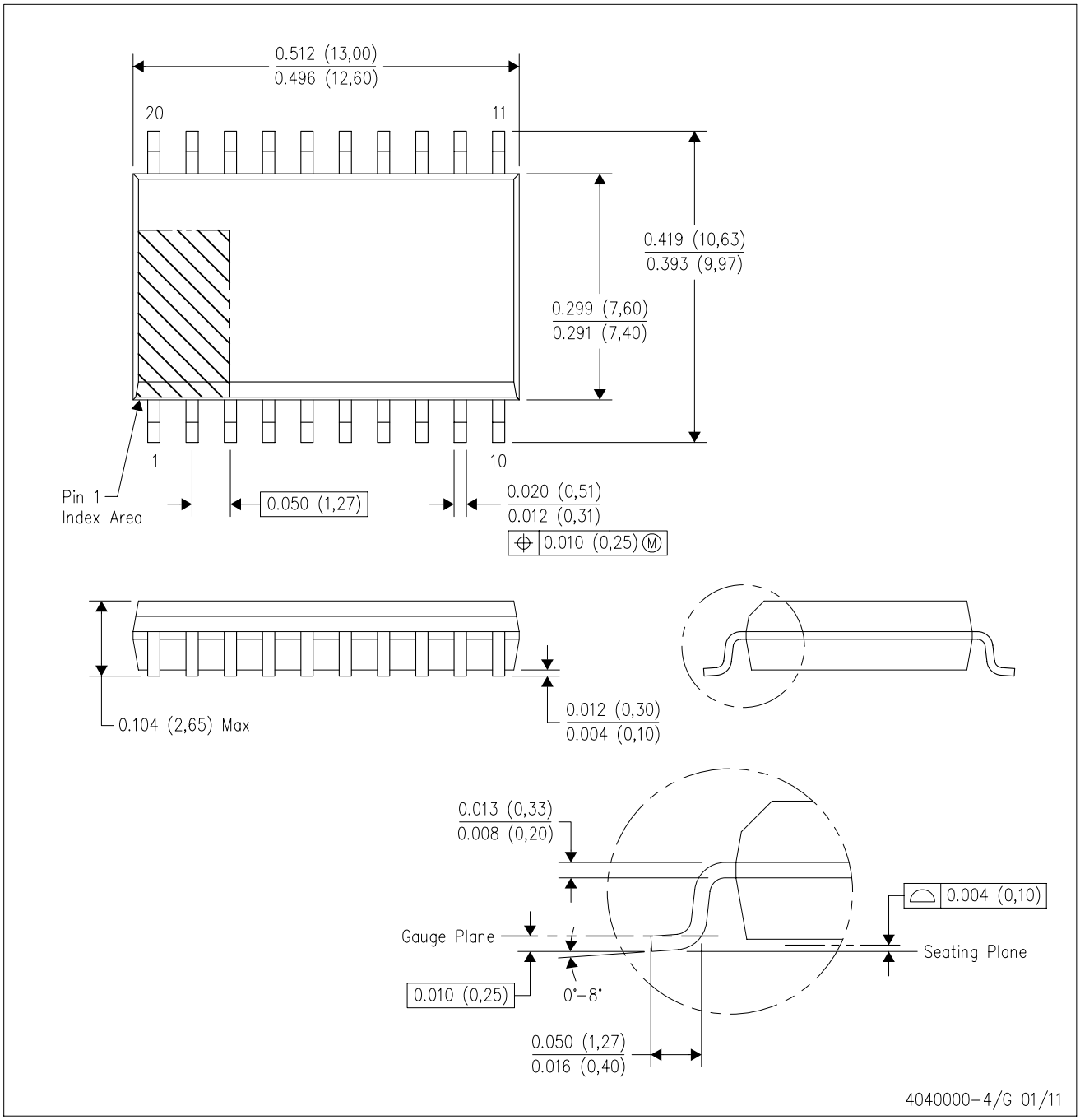
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

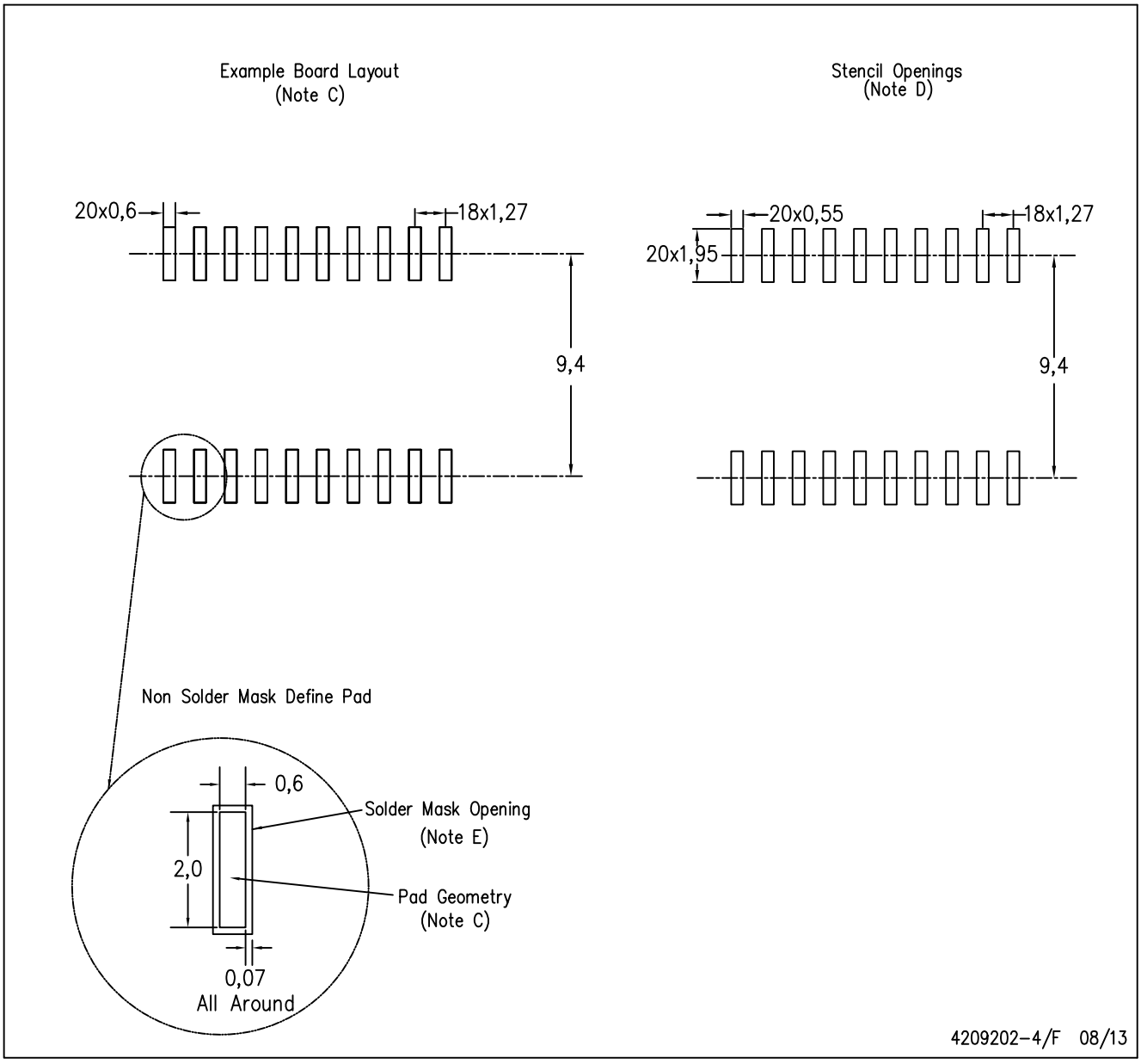
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC6C5912QDWRQ1	SOIC	DW	20	2000	367.0	367.0	45.0
TLC6C5912QPWRQ1	TSSOP	PW	20	2000	367.0	367.0	38.0

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



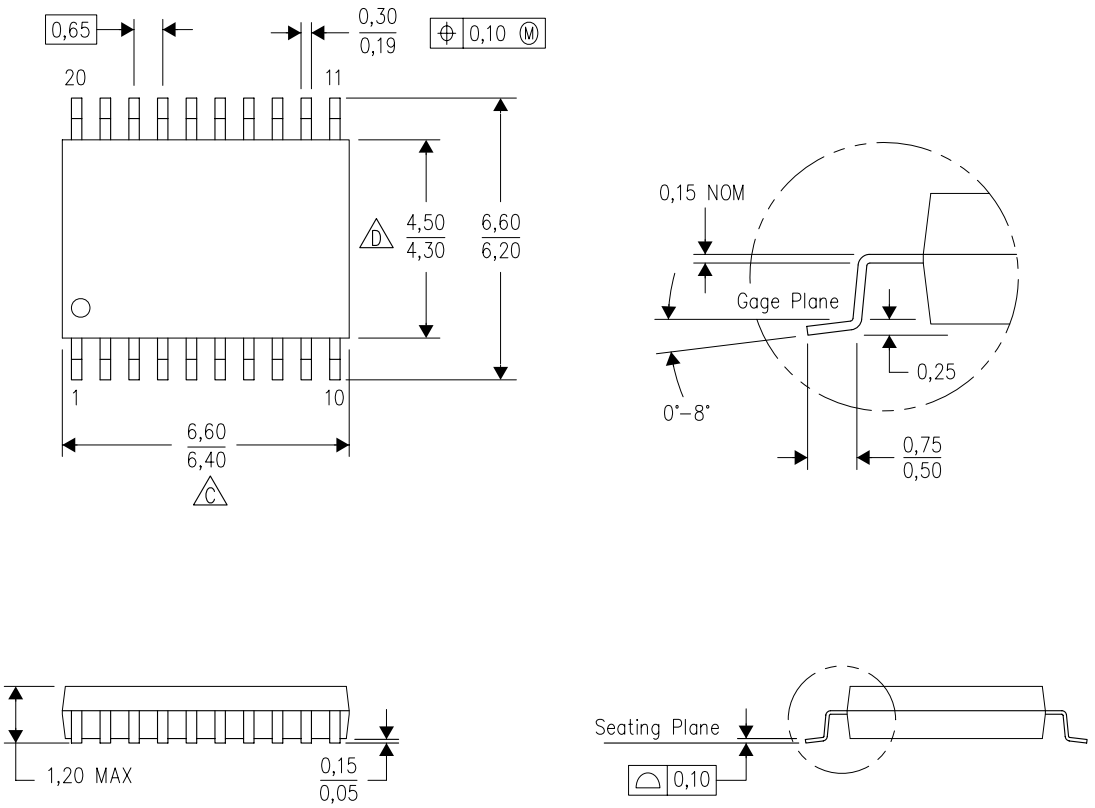
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

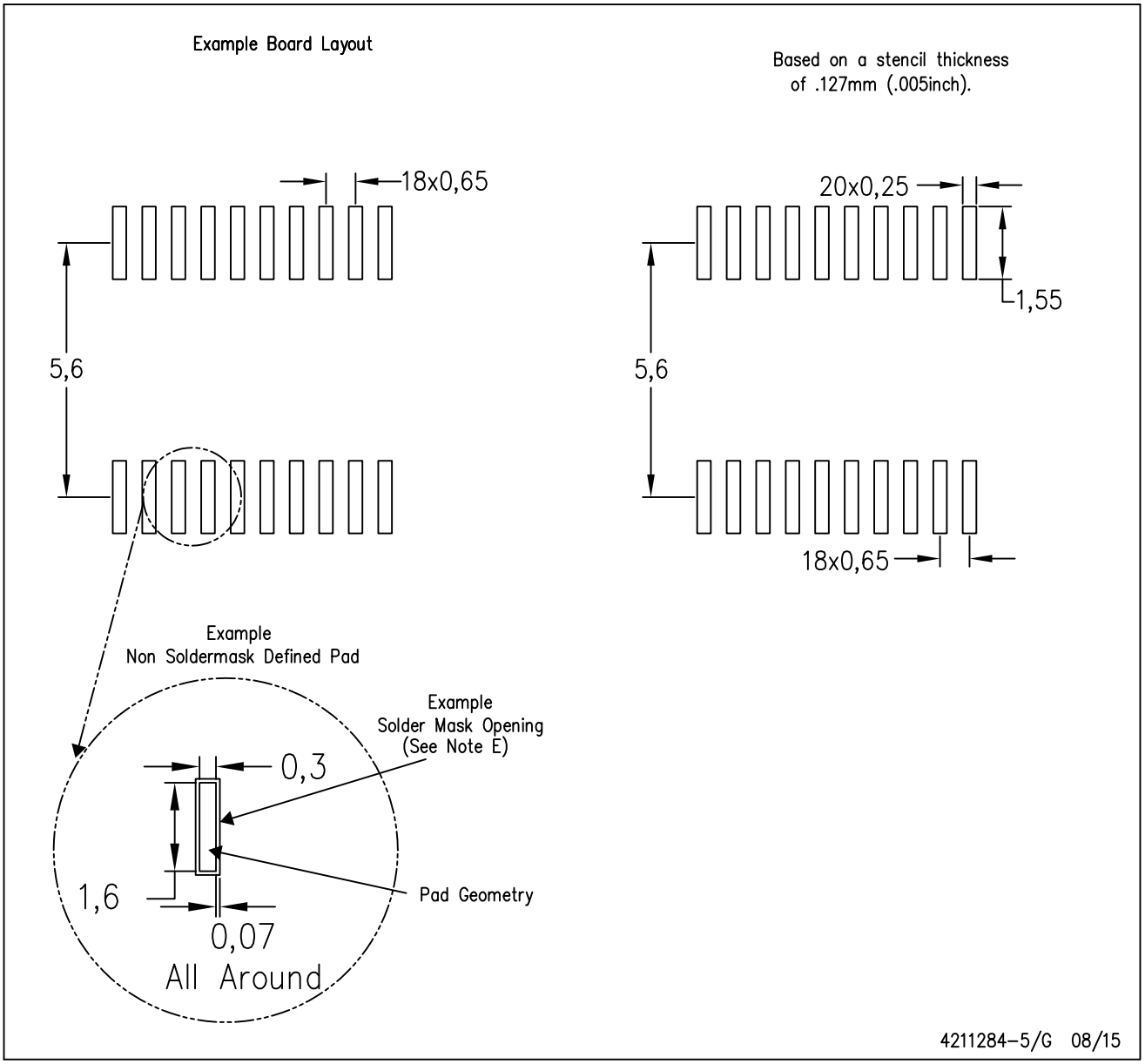
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265